DESIGNER'S NOTEBOOK

Who needs to bother winding miles of wire onto a bobbin when high voltages can be generated with some inverters and a handful of diodes and capacitors? Rory Holmes shows how it's done.

In this month's first Designer's Notebook we shall be looking at a variety of interesting voltage multiplier circuits that can be built using ordinary CMOS gates and common-or-garden 1N4148 signal diodes. DC-to-DC converters for a number of applications became possible by simply driving voltage multiplier chains with an AC clock signal, again implemented with CMOS gates. The initial supply voltage can be multiplied both positively and negatively, to give for example a split rail op-amp supply from a standard 5 V TTl supply. Negative and positive voltage references used in analogue-to-digital conversion and other signal conditioning circuits can also be generated, as can general purpose high voltage bias rails.

By using a novel 'chain' of inverter gates to independently drive each node of a diode-capacitor ladder, some rather unique circuits result.

Chain Reaction

First, let's look at the usual multiplier circuits shown in Fig. 1a. These are normally used with rectifier-type diodes, low frequency AC inputs (sine waves) from transformers, and electrolytic smoothing capacitors. At first glance there seems to be no common pattern between them, and little similarity to the multiplier chains used in TVs and other EHT power supplies.

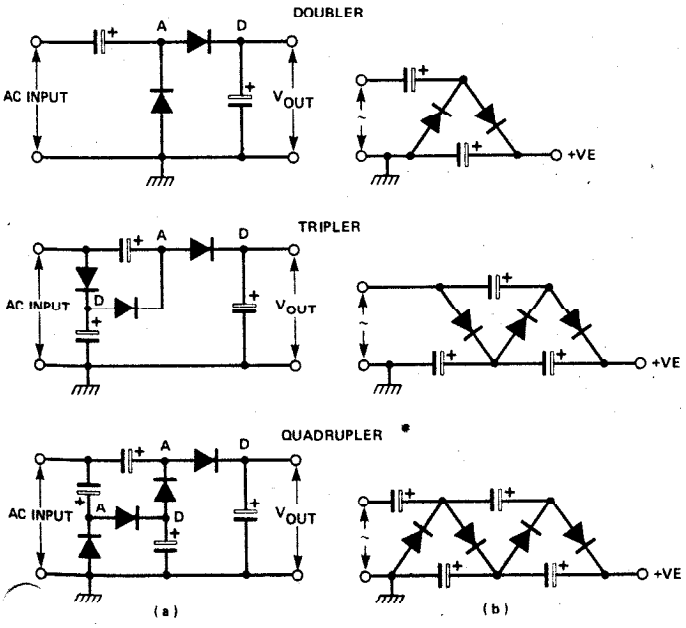

Fig. 1 Standard voltage multiplier circuits.

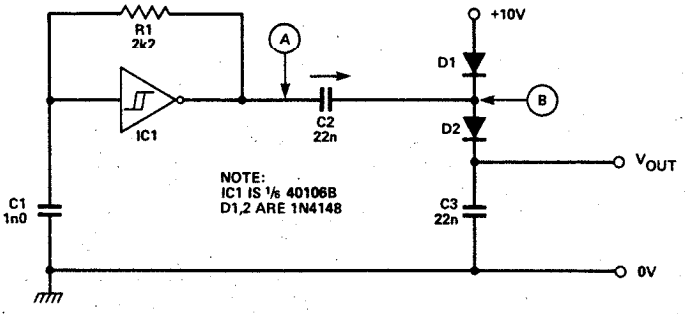

Fig. 2 A CMOS doubler circuit.

However, in all cases the AC input waveform is fed via capacitors to appear at those circuit junctions marked 'A' in Fig. 1a, while those junctions marked 'D' will maintain a steady DC potential relative to the earth point. We can thus redraw the circuits by connecting up the capacitors in two series chains (assuming their values are altered accordingly) and still preserve the same circuit action. One chain carries the AC signal, while the other accumulates the DC voltage shifts. Figure 1b shows these redrawn circuits, which now appear as extensions of the standard ladder network. The doubler, of course, remains in its original form since it only has one set of capacitors.

Starting with the doubler, we can build a very simple DC-to-DC converter using one CMOS gate as shown in Fig. 2. The Schmitt inverter gate is configured as a square wave oscillator running at about 100 kHz — the multiplier capacitors C2 and C3 will therefore have a low impedance at this frequency, which is also within the switching speed capability of the 1N4148s. For this reason, rectifier diodes such as the 1N4001, which have much slower switching speeds, cannot be used in these circuits.

The oscillator output at point 'A' will therefore be switching between the 0 V and 10 V supply levels. When the output is at logic low, capacitor C2 will charge up positively (in the direction of the arrow) via D1. D2 is reverse biased and so effectively out of circuit. When point 'A' goes high to +10 V the positive end of C2 at 'B' will be raised to +20 V. This reverse biases D1 and allows C3 to charge up through D2. The voltage on C3 is thus maintained at about +20 V less two diode drops (ie at 18V6) as the cycle repeats itself. This is known as a diode charge pump.

Building An Extension

This principle can be extended using exactly the same chainlike structure as illustrated in the positive and negative multipliers of Fig. 3. In both cases the inverter gates are cascaded and driven from a square wave

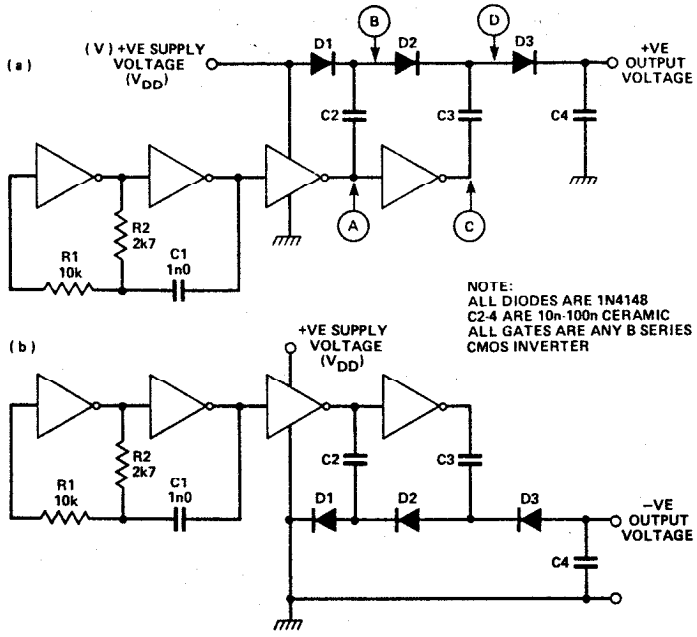

Fig. 3a A two-stage positive voltage multiplier (multiples by +3). b. A two-stage negative voltage multiplier (multiplies by −2).

oscillator at around 100 kHz. Each inverter gate contributes its own output current (a maximum of around 2 mA) via the capacitors into the multiplier chain: because of this, the available output current will always be the same no matter how many times the voltage is multiplied (two times in this case).

The positive multiplier output of Fig. 3a includes the initial positive supply potential, and so generates three times this voltage less the three diode drops of 0V7 each. The negative multiplier of Fig. 3b, on the other hand, is referenced to the ground rail, giving −2 times the voltage (again less the diode drops).

As mentioned before, all the diodes are 1N4148s: the multiplier capacitors C2-4 are all non-critical and may be anything from 10nF to 100nF. C4 may be a polarised tantalum capacitor of a few microfarads to provide further smoothing. Any type of CMOS gate which can be connected as an inverter could be used, as well as all the standard inverters, though the 4049B hex inverter offers slightly more output current. It's also possible to use the 74C series types such as the 74C04 or 74C14. Pin-outs for these chips are given in Fig. 4 and not on any of the circuit diagrams, since they differ from type to type.

The oscillator implementation and its frequency are also non-critical; you could experiment with anything

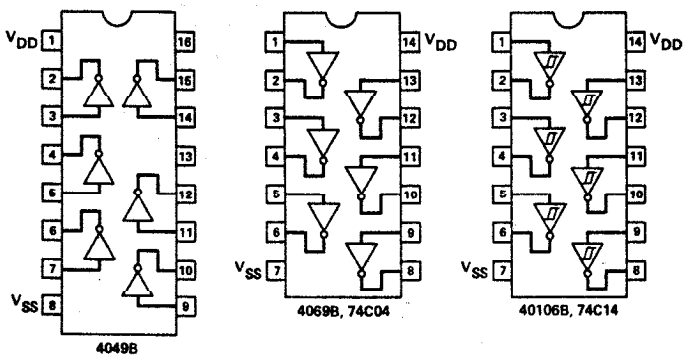

Fig. 4 Pin-outs for the standard hex inverter packages which may be used in the circuits given in this article.

from several kilohertz to several hundred kilohertz. Remember, though, that as the frequency decreases, the impedance for a given capacitor value will increase, so increasing the impedance of the multiplier output.

Table 1 lists out the different voltages you can expect from different chain lengths and supply voltages, based on the circuits of Fig. 3. The number of stages refers to the number of capacitors that are actively driven from inverter outputs. Using this table it becomes very easy to design a generator for any voltage requirement; the output voltage could be clamped to the exact level required using an ordinary zener diode regulator. But remember there isn't much current available, and as the output is loaded the voltage will decrease due to the supply impedance. The higher supply voltages will generally provide more output current.

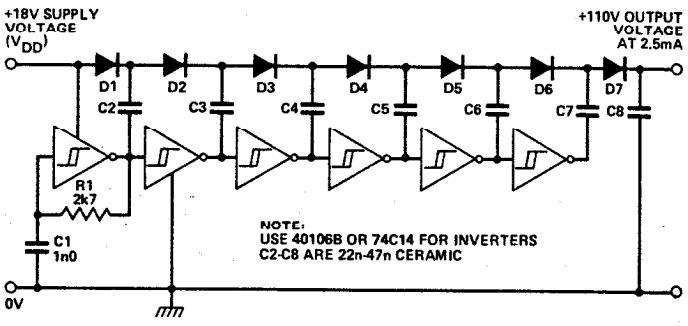

Fig. 5 A 110 V supply using one hex inverter IC.

As an example, Fig. 5 shows a longer multiplier designed to give 110 V and built using only one hex inverter IC, of the Schmitt trigger type (40106B). Using ceramic capacitors, this circuit could be built to a very small size.

Operating Principles

How do these multipliers actually work — the doubler circuit of Fig. 2 is straightforward, but what about the longer types? Voltage multiplier explanations are usually notoriously difficult to follow, let alone understand, and

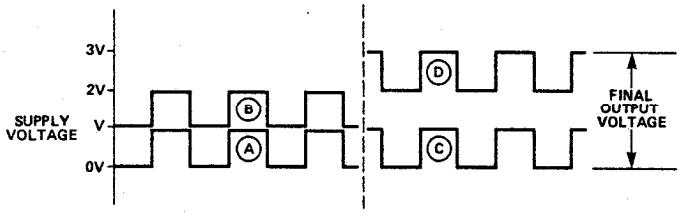

Fig. 6 Waveforms for a two-stage positive multiplier (idealised for clarity with diode drops ignored).

we shall therefore adopt a more graphic approach. If we measure the voltages at the lettered points in Fig. 3a and plot them against time, we get the waveforms shown in Fig. 6. These waveforms have been idealised for clarity — no account has been taken of the voltage drops due to the diodes in the circuit. From these it can be seen that the voltage across C2 (the difference between the waveforms A and B) is a constant 1V, where V is the supply voltage, while that across capacitor C3 (between points C and D) is 2V. We also know that the final output voltage across C4 is 3V. Moving down the chain towards the final output, then, we find that each capacitor maintains a DC charge which increases in integer multiples of the supply voltage. How so?

Consider capacitor C2 in Fig. 3a. At power-on it is discharged but when point A switches low, it charges up

TABLE 1

OUTPUT POLARITY / NO. OF STAGES	CMOS SUPPLY VOLTAGE 5V +	5V −	10V +	10V −	18V +	18V −
1	8.6	3.6	18.6	8.6	34.6	16.6
2	12.9	7.9	27.9	17.9	51.9	33.9
3	17.2	12.2	37.2	27.2	69.2	51.2
4	21.5	16.5	46.5	36.5	86.5	68.5
5	25.8	20.8	55.8	45.8	103.8	85.8
6	30.1	25.1	65.1	55.1	121.1	103.1
7	34.4	29.4	74.4	64.4	138.4	120.4

Table relating supply voltage and number of stages to the (unloaded) output voltage, for positive and negative output multipliers based on the circuits of Figs. 3a and 3b and allowing 0V7 for each diode drop.

to the supply voltage via D1 (neglecting diode drops). Point B is therefore at supply voltage. When point A switches high, then, point B is raised to twice the supply voltage. Point C must be at zero volts since it is the inverse of point A, so current flows via D2 (which is now forward iased) from point B into C3 until C3 is charged up to the .oltage at B (ie twice supply). The next clock pulse takes point A low, so point B is at supply less the voltage that has leaked into C3, and C2 is topped up via D1 again. Meanwhile point C has switched to supply voltage, so point D is now at three times supply and D2 is reverse biased, preventing C3 from discharging back into C2. C3 can discharge into C4 via D3, however, so the voltage across C4 is maintained at three times supply.

It should now be clear that no matter what the length of the multiplier, each capacitor in the chain maintains a steady DC charge which equals that on the previous one plus the supply voltage, and each capacitor tops up the next one in the chain on each alternate half-cycle. Figure 7a, for example, shows five stages of a multiplier chain driven by a square wave signal, while Figs. 7b and 7c use a waveform to represent the voltage levels at each capacitor node for each half of the cycle. The direction and voltage of the DC charges on each capacitor is also shown — remember these are constant as shown by the graph of Fig. 6.

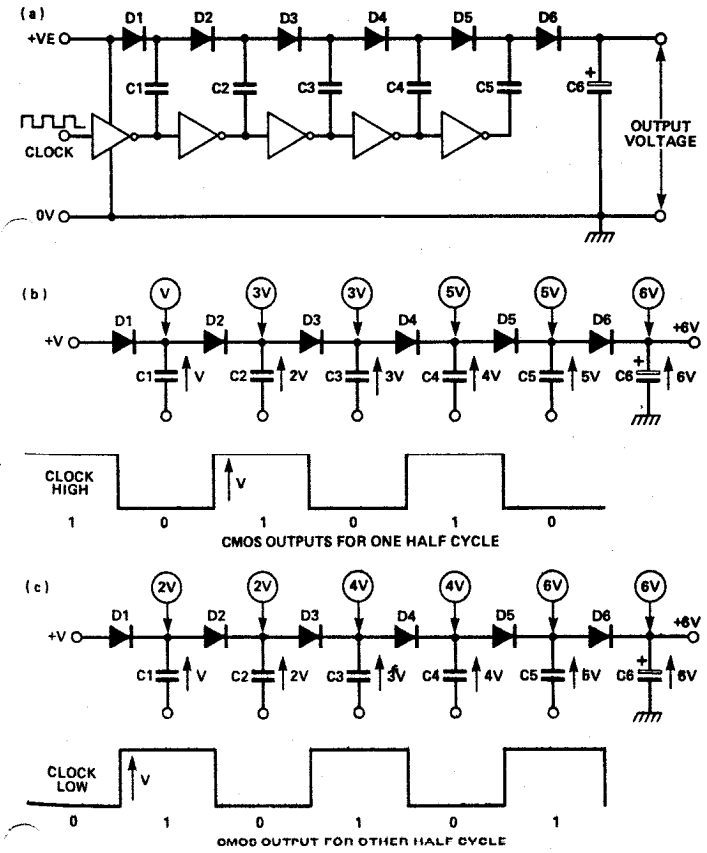

Fig. 7 How multiplier voltages accumulate down the chain.

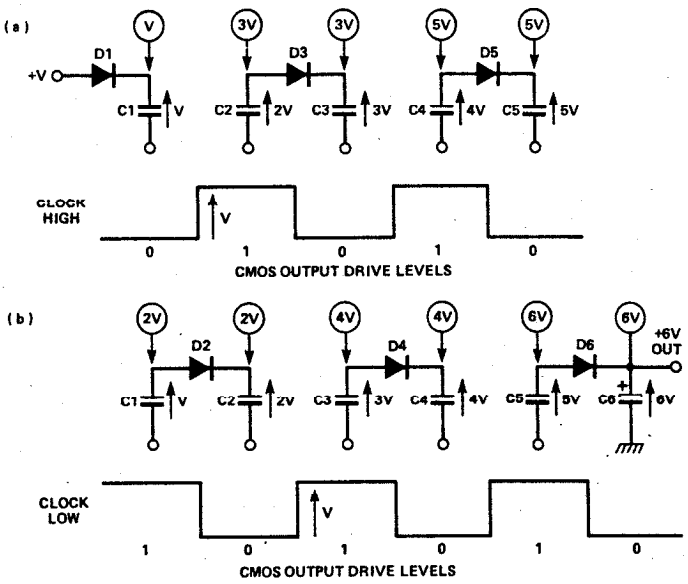

Fig. 8 Charging paths for an extended multiplier chain. The diagrams only show those diodes which are forward biased (conducting) during alternate half cycles of the drive waveform.

Looking at C1 and C2 in Fig. 7b we can see that the positive (top) end of C1 will be at V volts (V is the supply voltage) while the positive end of C2 is at 3V volts (2V of its own, raised up a further V volts at the CMOS output). Diode D2 will therefore be reversed biased and effectively out of circuit. For similar reasons C3 will be at 3V volts (less that which has leaked away) and can therefore be charged up via D3 from C2. On the other half cycle in Fig. 7c, however, C3 will be raised up to 4V volts by the CMOS output, while C2 returns to 2V. So this time D3 is reverse biased and will not conduct. C1 is now raised to 2V and can thus charge C2 via D2. The conducting and non-conducting parts of the circuit for each half cycle are shown in Fig. 8, which gives a much clearer illustration of the diode charge pump action.

The Appliance Of Science

Figure 9 shows the circuit of a split-rail power supply that generates ±10 V from a 5 V supply input. It could be

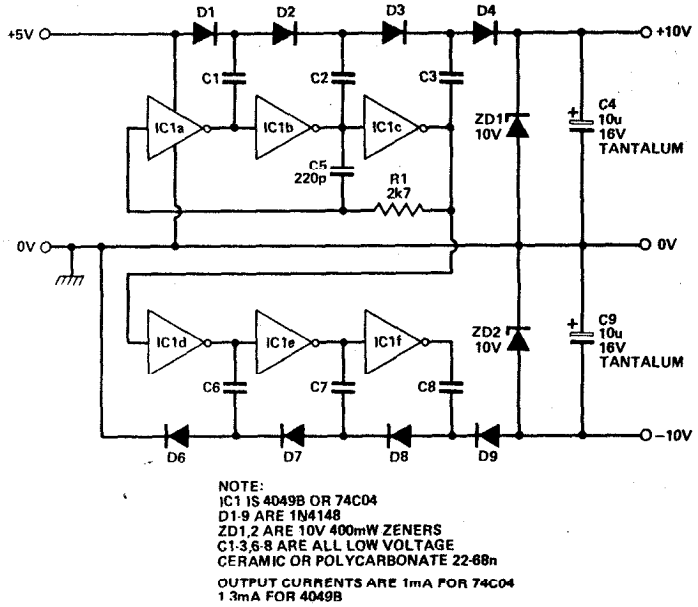

Fig. 9 A split-rail supply using one hex inverter package.

used to power low current op-amp circuitry and other CMOS circuits from a standard TTL power supply. Again, only one hex inverter pack is required and we recommend that the 4049B is used with its slightly higher output current capability. The circuit takes advantage of the three cascaded inverters that drive the positive multiplier chain, by also using them to form a 'ring-of-three' oscillator. The multiplier chain is therefore self-oscillating!

The positive side in turn drives the negative chain of IC1d, e and f. From Table 1 we would expect the available output voltages to be +17V2 and −12V2, which are then clamped to the ±10 V levels by zeners ZD1 and ZD2. Series limiting resistors for the zener diodes are unnecessary due to the current-limited output of the multiplier.

Figure 10 shows a variation on the previous circuit's positive multiplier section, using all six inverters to provide more output current at ±10 V. To achieve higher output currents, simply parallel the CMOS gates that drive the capacitor chain: the available currents will add together due to the nature of the CMOS output FETs. This technique is useful for CMOS operating at low supply voltages.

Figure 11 gives the circuit for a 24-stage positive multiplier to generate a high-voltage, low-current supply. This could be used for a solid state 'megger' (high resistance meter and insulation tester). The 24 stages can be achieved using only four hex inverter packs, and will provide 433 V from an 18 V supply. This circuit illustrates the fact that the inverters may be wired up in any fashion so long as alternate capacitors receive opposite phases of the square wave.

The circuit will deliver at least 2 mA at 430 V! — not lethal but pretty painful, so be careful. We suggest the addition of a 1M0 series resistor in the positive supply lead to limit the available current to about 400 uA. A 100 uA meter would provide suitable megohm readings.

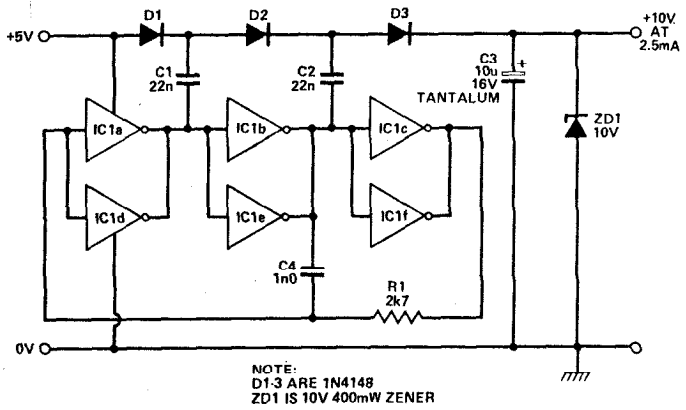

Fig. 10 Paralleling inverter stages to give a higher current supply.

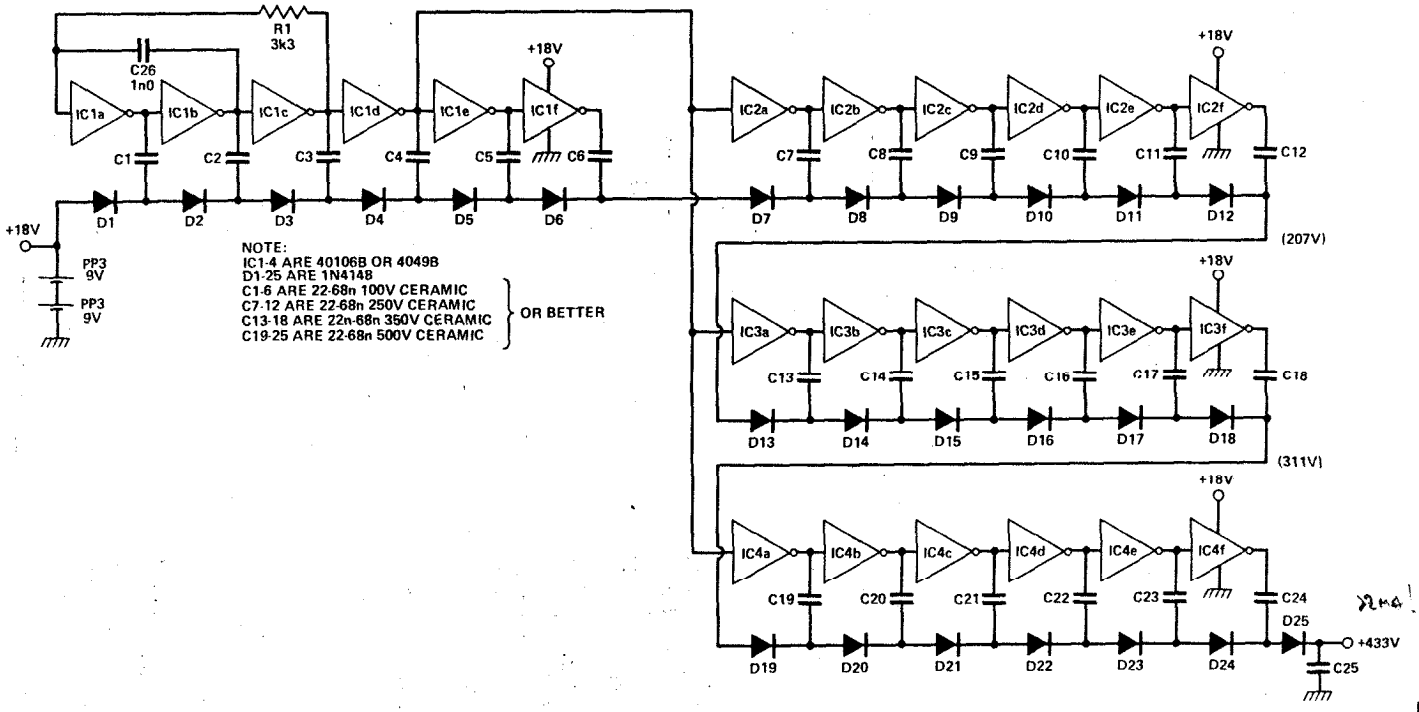

Fig. 11 A 433 V generator using a 24-stage positive multiplier and an 18 V supply.

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